TB-FMCH-HDMI4K
Hardware User Manual

Rev.2.02

Revision History

Version	Date	Description	Publisher
1.00	2014/12/29	Initial release	JC
2.00	2015/06/30	Updated. Released.	ST
2.01	2015/08/10	-Updated support web link on page 8 -removed table link on page 28 -Updated Xilinx support link on page 29 -Add high light jumper setting on page 33 -Add note on page 18 and 20	MY
2.02	2016/01/13	Delete Table2-1	MY

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Introduction

Thank you for purchasing the **TB-FMCH-HDMI4K** board. Before using the product, be sure to carefully read this user manual and fully understand how to correctly use the product. First read through this manual, and then always keep it handy.

SAFETY PRECAUTIONS

Be sure to observe these precautions!

Observe the precautions listed below to prevent injuries to you or other personnel or damage to property.

- **Before using the product, read these safety precautions carefully to assure correct use.**
- **These precautions contain serious safety instructions that must be observed.**
- **After reading through this manual, be sure to always keep it handy.**

The following conventions are used to indicate the possibility of injury/damage and classify precautions if the product is handled incorrectly.

Danger	Indicates the high possibility of serious injury or death if the product is handled incorrectly.
Warning	Indicates the possibility of serious injury or death if the product is handled incorrectly.
Caution	Indicates the possibility of injury or physical damage in connection with houses or household goods if the product is handled incorrectly.

The following graphical symbols are used to indicate and classify precautions in this manual.
(Examples)

	Turn off the power switch.
	Do not disassemble the product.
	Do not attempt this.

Warning	
	**In the event of a failure, disconnect the power supply.** If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately and contact our sales personnel for repair.
	**If an unpleasant smell or smoking occurs, disconnect the power supply.** If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately. After verifying that there is no smoking, contact our sales personnel for repair.
	**Do not disassemble, repair or modify the product.** Otherwise, a fire or electric shock may occur due to a short circuit or heat generation. For inspection, modification or repair, contact our sales personnel.
	**Do not touch a cooling fan.** As a cooling fan rotates at high speed, do not put your hand close to it. Otherwise, it may cause injury to persons. Never touch a rotating cooling fan.
	**Do not place the product on unstable locations.** Otherwise, it may drop or fall, resulting in injury to persons or failure.
	**If the product is dropped or damaged, do not use it as is.** Otherwise, a fire or electric shock may occur.
	**Do not touch the product with a metallic object.** Otherwise, a fire or electric shock may occur.
	**Do not place the product in dusty or humid locations or where water may splash.** Otherwise, a fire or electric shock may occur.
	**Do not get the product wet or touch it with a wet hand.** Otherwise, the product may break down or it may cause a fire, smoking or electric shock.
	**Do not touch a connector on the product (gold-plated portion).** Otherwise, the surface of a connector may be contaminated with sweat or skin oil, resulting in contact failure of a connector or it may cause a malfunction, fire or electric shock due to static electricity.

Caution	
	Do not use or place the product in the following locations. • Humid and dusty locations • Airless locations such as closet or bookshelf • Locations which receive oily smoke or steam • Locations exposed to direct sunlight • Locations close to heating equipment • Closed inside of a car where the temperature becomes high • Static-prone locations • Locations close to water or chemicals Otherwise, a fire, electric shock, accident or deformation may occur due to a short circuit or heat generation.
	Do not place heavy things on the product. Otherwise, the product may be damaged.

■ Disclaimer

This product is a HDMI interface for Xilinx FPGA evaluation boards. Tokyo Electron Device Limited assumes no responsibility for any damages resulting from the use of this product for purposes other than those stated.

Even if the product is used properly, Tokyo Electron Device Limited assumes no responsibility for any damages caused by:

(1) Earthquake, thunder, natural disaster or fire resulting from the use beyond our responsibility, acts by a third party or other accidents, the customer's willful or accidental misuse, or use under other abnormal conditions.
(2) Secondary impact arising from use of this product or its unusable state (business interruption or others)
(3) Use of this product against the instructions given in this manual.
(4) Malfunctions due to connection to other devices.

Tokyo Electron Device Limited assumes no responsibility or liability for:

(1) Erasure or corruption of data arising from use of this product.
(2) Any consequences or other abnormalities arising from use of this product, or
(3) Damage of this product not due to our responsibility or failure due to modification.

This product has been developed by assuming its use for research, testing or evaluation. It is not authorized for use in any system or application that requires high reliability.
Repair of this product is carried out by replacing it on a chargeable basis, not repairing the faulty devices. However, non-chargeable replacement is offered for initial failure if such notification is received within two weeks after delivery of the product.
The specification of this product is subject to change without prior notice.
The product is subject to discontinuation without prior notice.

1. Related Documents and Accessories

All documents relating to this board can be downloaded from the TED Support Web at address
https://www.teldevice.co.jp/spweb/c0208s

Table 1-1 Accessories

Description	Manufacturer	Quantity
Spacer, 10mm, M2.6	Hirosugi	2
Spacer, 10mm w/ screw, M2.6	Hirosugi	4
Spacer, 25mm, M2.6	Hirosugi	2
Screw, 6mm, M2.6 w/ washers	Hirosugi	6

2. Overview

The TB-FMCH-HDMI4K is functionally divided into a source circuit and a sink circuit. Each side is designed to be compatible with the HDMI 2.0 specification, with an individual TMDS channel throughput of up to 6 Gbps thus enabling support of 4K resolution at 60fps. The source circuit is based on the Texas Instruments SN65DP159 D++ to TMDS Retimer.

The TB-FMCH-HDMI4K has demonstrated operation up to 4096x2160p 60Hz.
For the latest support resolution, please refer to the following Xilinx HDMI IP web page.
http://www.xilinx.com/products/intellectual-property/hdmi.html

The TB-FMCH-HDMI4K utilizes HDMI Type-A receptacles and Samtec's FMC HPC connector for connection to a platform board having a High-Pin Count (HPC) connector.
Physically, this FMC is a single width air-cooled card that is compatible with the ANSI/VITA 57.1 FPGA Mezzanine Card (FMC) Standard.
The Display Data Channel (DDC) and Consumer Electronics Control (CEC) are supported. An I2C controlled clock multiplier/generator is included to produce a reference frequency of up to 346MHz.

A second FMC HPC connector allows a second TB-FMCH-HDMI4K to be stacked to expand to two source and two sink circuits.

Note: Only stack FMCs that are identical (i.e. same part number and same revision). Do not attempt to stack different FMCs. Stacking FMCs of different types or revisions could cause damage.

Note: Due to I/O constraints on the FMC connector there are restrictions on the capabilities of the stacked FMC:

a. The HDMI sink clock on the second extender FMC is not connected to the J3 FMC main board connector. This practically limits the sink operation of the stacked FMC to the same sink clock frequency as the primary FMC and generally the same traceable source to avoid clock slipping.
b. Due to I/O limitations on the J3 Main Board FMC connector, the stacked FMC's Si5324A clock generator only provides EX_CLK_LVDS_P/N to the J8 connector. This

may or may not limit functionality (IP core dependent).

Note: The TB-FMCH-HDMI4k does not support the HDMI Ethernet and Audio Return Channel (HEAC) on either HDMI interface.

Note: VIO_B_M2C is directly connected to 3P3V. User is responsible for making sure that the carrier card can accept a VIO_B_M2C of 3.3V nominal.

3. Features

HDMI Source Device	Texas Instruments SN65DP159RSB
FMC Main Connector	Samtec ASP-134488-01
FMC Extender Connector	Samtec ASP-134486-01
HDMI Connectors	Samtec HDMR-19-01-S-SM
FPGA GPIO Signal Level	1.2V through 3.3V using voltage level translators or AC coupling
Clock Multiplier/Generator	Silicon Labs Si5324C-C-GM

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND
2	GND	CLK3_BIDIR_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND
			LPC Connector	LPC Connector			LPC Connector	LPC Connector		

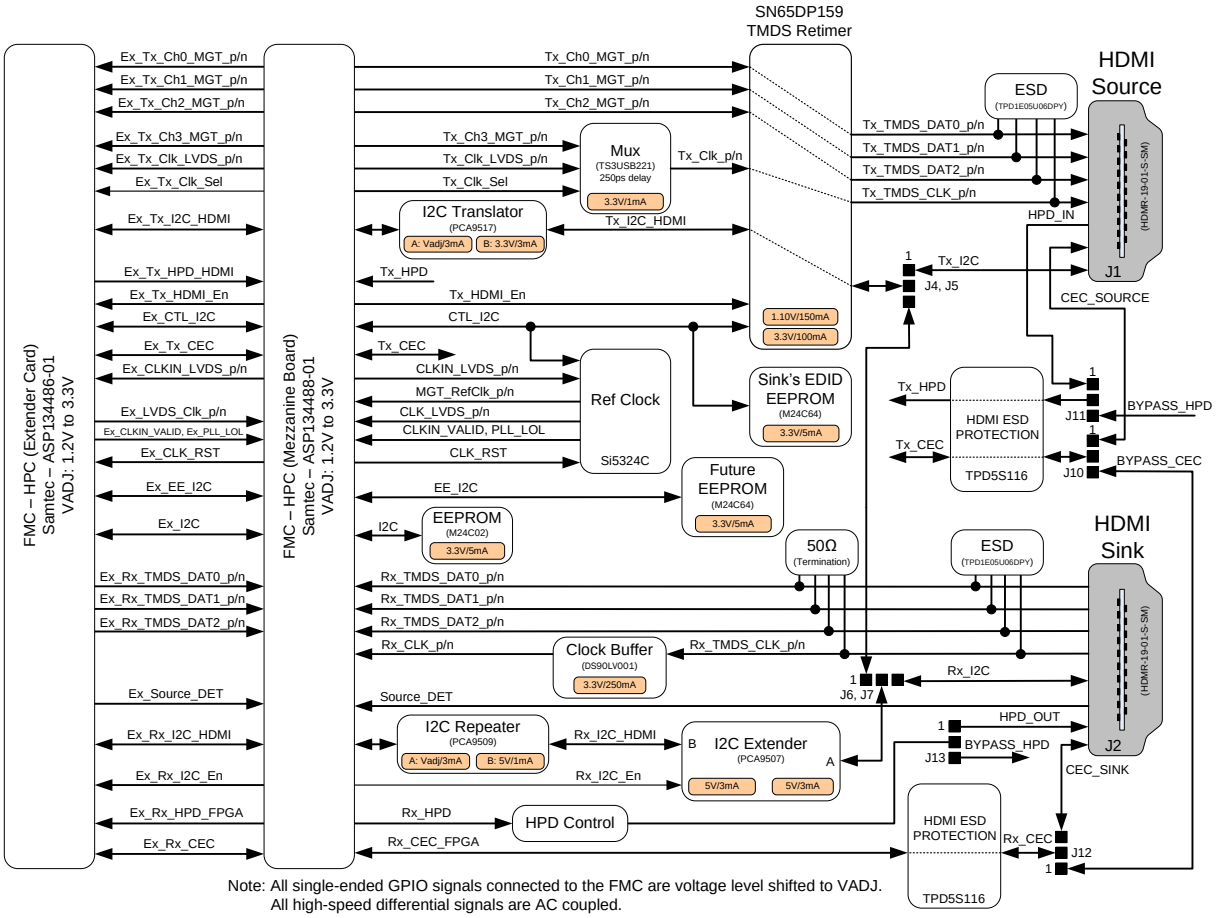
Figure 3-1 FMC HPC Connector Pin Layout as per VITA 57.1

4. Block Diagram

Figure 4-1 shows the TB-FMCH-HDMI4K block diagram.

The FMC-HPC main connector is mounted on the component side of the board.

The FMC-HPC extender connector is mounted coincident with the main connector on the opposite side of the board. Voltage level translators are not shown in the block diagram.



Note: All single-ended GPIO signals connected to the FMC are voltage level shifted to VADJ.
All high-speed differential signals are AC coupled.

Figure 4-1 TB-FMCH-HDMI4K Block Diagram

5. External View of the Board

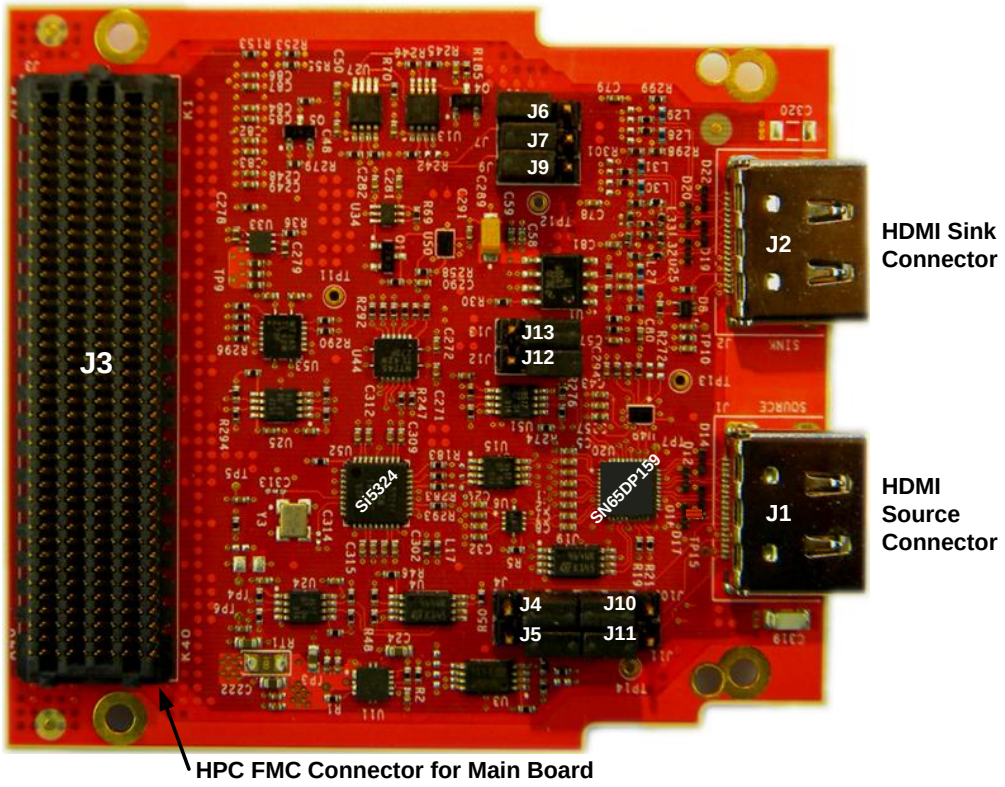


Figure 5-1 External View of TB-FMCH-HDMI4K (Component Side)

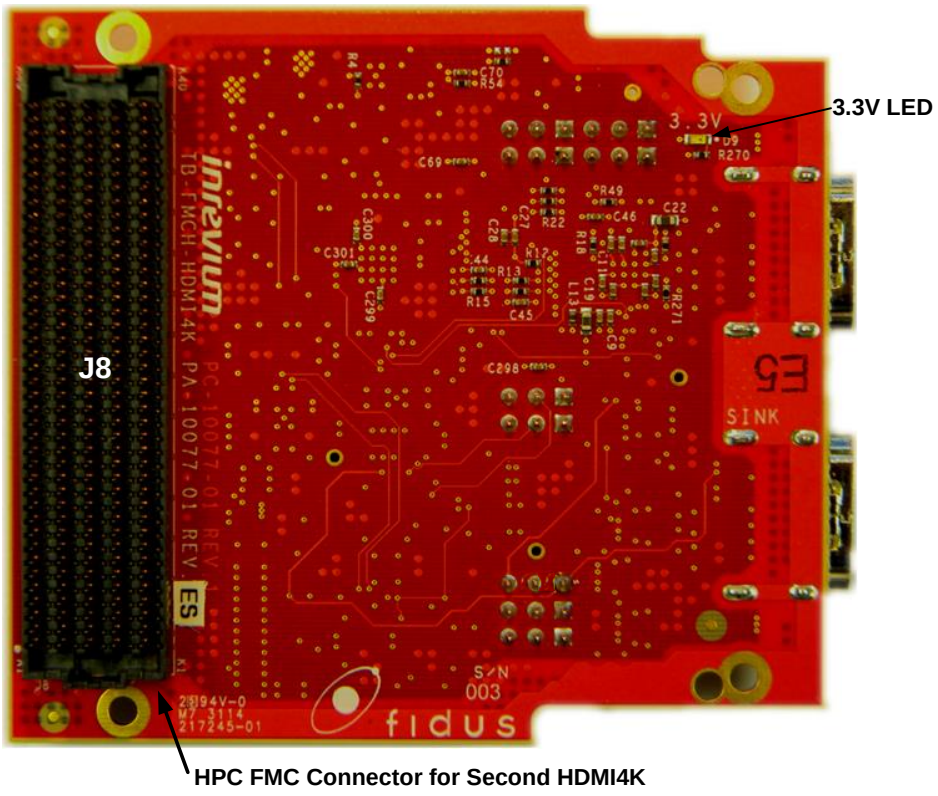


Figure 5-2 External View of TB-FMCH-HDMI4K (Solder Side)

6. Board Specification

The following shows the TB-FMCH-HDMI4K board physical specifications.

External Dimensions	76.50 mm long x 69.00 mm wide
Number of Layers	10 layers
Board Thickness	1.6 mm
Material	Megtron 4
FMC Main Connector	Samtec ASP-134488-01
FMC Extender Connector	Samtec ASP-134486-01
HDMI Connectors	Samtec HDMR-19-01-S-SM

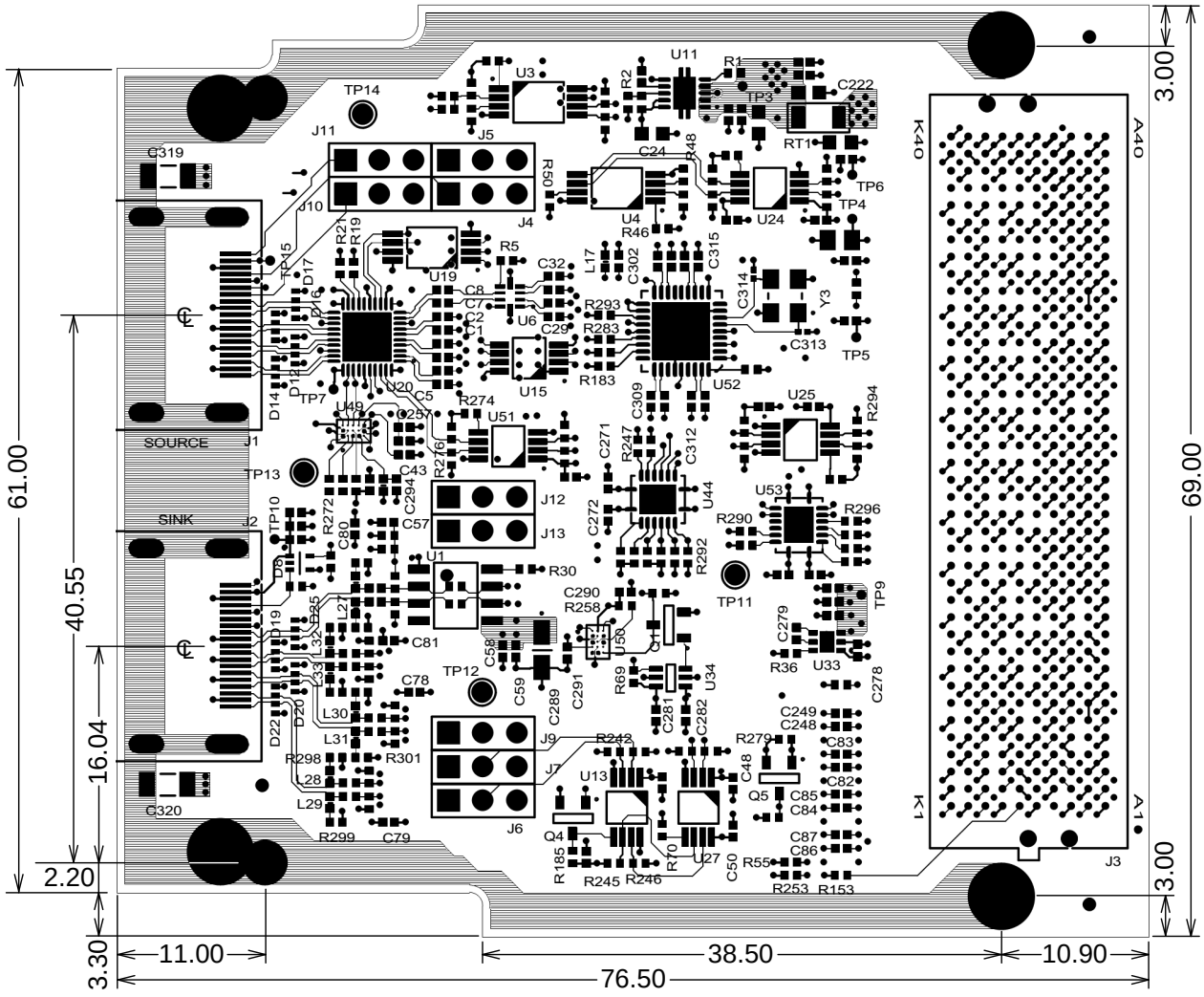


Figure 6-1 TB-FMCH-HDMI4K Board Dimensions (mm)

7. Supplying Power to the Board

Figure 7-1 shows the TB-FMCH-HDMI4K power supply structure. There is one LDO regulator to generate 1.1 volts for the SN65DP159 and one switching regulator for 5.0 volts. Both use 3.3 volts from the carrier card to generate the lower voltages. The carrier card 12 volts rail is not used. VADJ can be from 1.2V to 3.3V and is used mainly for voltage translators and I2C repeaters. There is no onboard power sequencing.

A green LED, located on the solder side, indicates the presence of the VCC_3V3 rail. Since this rail is the main power source for the card it is protected with a 1.5 amp PTC resettable fuse (600mA is the maximum expected current draw). If this fuse trips due to an overcurrent fault remove power to the card and wait a few minutes for the PTC to cool. Remove the condition causing the excess current and apply power. If the PTC trips again, remove power, wait for the fuse to cool, remove the card from the carrier, and contact inrevium technical support.

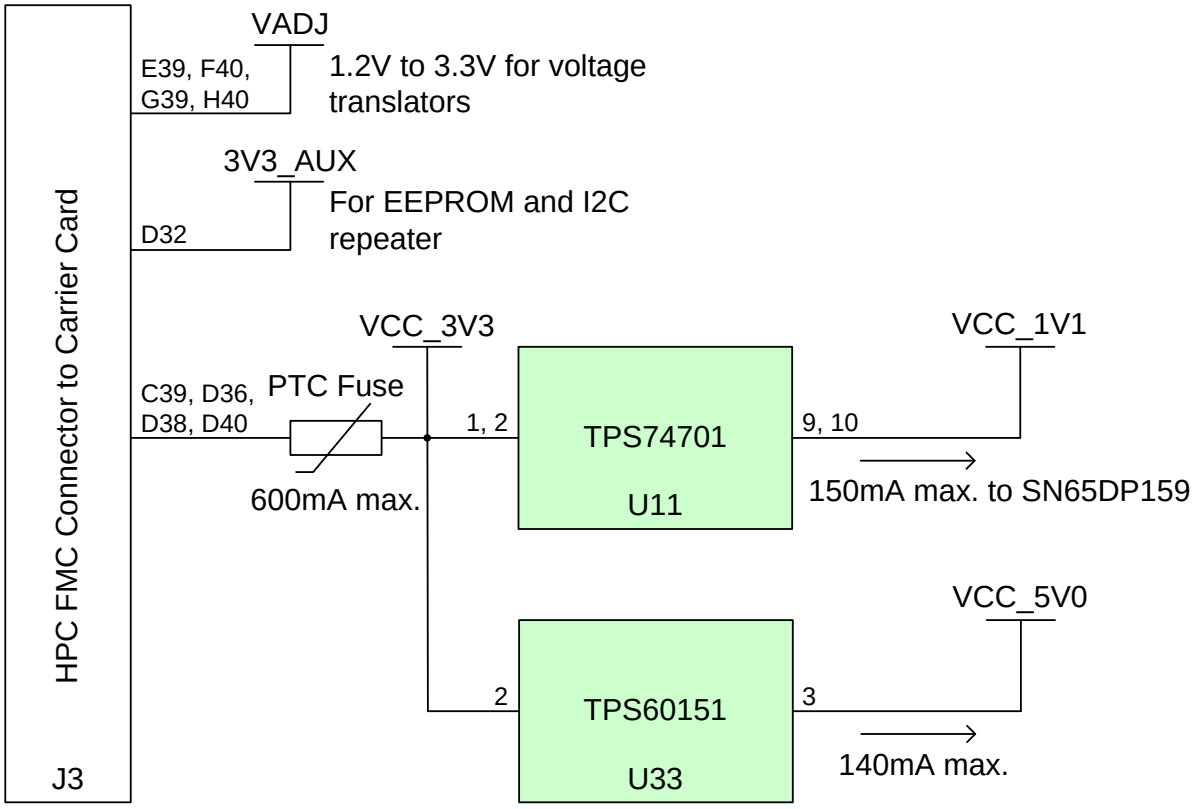


Figure 7-1 TB-FMCH-HDMI4K Power Supply Structure

7.1. HDMI Five Volts Power

The HDMI source connector power is supplied from the TPS60151 boost switching regulator through a Texas Instruments TPD5S116 HDMI companion device. This device provides transient and current protection at the connector. The HDMI sink connector input five volts also goes to a TPD5S116 for protection via a three-pin header (J9). J9 is used to internally supply five volts to the sink circuits if five volts is not available at the sink connector, such as when the HDMI cable is disconnected. Figure 7-2

shows the HDMI source and sink five volts connections.

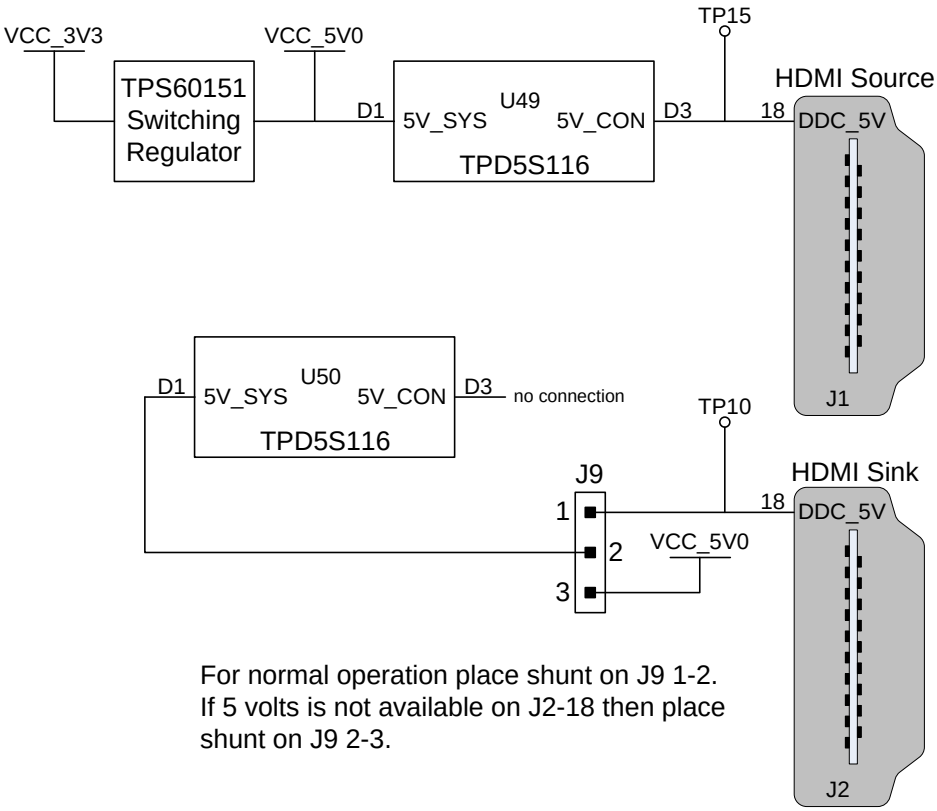


Figure 7-2 HDMI Source and Sink 5 Volts Supplies

8. Connectors

There are four connectors on the FMC. One HPC FMC connector provides connectivity to the Main Board (J3) and another HPC FMC connector (J8) is for a second (stacked) TB-FMCH-HDMI4K, enabling additional HDMI source and sink ports. The other two connectors are the HDMI source and sink connectors, located on the front edge of the card.

Note: Only stack FMCs that are identical (i.e. same part number and same revision). Do not attempt to stack different FMCs. Stacking FMCs of different types or revisions could cause damage.

8.1. HPC FMC Connector to Main Board

The HPC FMC connector used to mate to the Main Board (carrier) is Samtec ASP-134488-01.

Table 8-1 shows the FMC connector pin assignment. In this table the C2M direction means carrier-to-mezzanine, which is thus, an input to the FMC. The M2C direction means mezzanine-to-carrier, which is thus, an output from the FMC. 'BI-DIR' means bi-directional, so the signal direction could be either an input or an output. Pins not included in the table are unconnected, including all HA[0:23] and HB[0:21] signals.

Table 8-1 HPC FMC Main Board Connector Pin Assignment

J3 Pin	Schematic Signal Name	VITA 57.1 Name	Direction	Type	Description
HDMI Source Signals					
C2	TX_CH0_MGT_P	DP0_C2M_P	C2M	CML	SN65DP159 channel 0 input
C3	TX_CH0_MGT_N	DP0_C2M_N			
A22	TX_CH1_MGT_P	DP1_C2M_P	C2M	CML	SN65DP159 channel 1 input
A23	TX_CH1_MGT_N	DP1_C2M_N			
A26	TX_CH2_MGT_P	DP2_C2M_P	C2M	CML	SN65DP159 channel 2 input
A27	TX_CH2_MGT_N	DP2_C2M_N			
A30	CLK_TX_CH3_MGT_P	DP3_C2M_P	C2M	CML	SN65DP159 1 of 2 clock mux input
A31	CLK_TX_CH3_MGT_N	DP3_C2M_N			
C26	CLK_TX_LVDS_P	LA27_P	C2M	LVDS	SN65DP159 2 of 2 clock mux input
C27	CLK_TX_LVDS_N	LA27_N			
C22	TX_CLK_SEL_FPGA	LA18_CC_P	C2M	LVTTL (VADJ)	SN65DP159 input clock mux select
C10	CLK_I2C_CTL_FPGA_SCL	LA06_P	C2M	LVTTL OD (VADJ)	I2C for Si5324, EDID EEPROM, and SN65DP159
C11	I2C_CTL_FPGA_SDA_OD	LA06_N	BI-DIR	LVTTL OD (VADJ)	
G33	TX_CEC	LA31_P	BI-DIR	LVTTL (VADJ)	Source CEC
G34	TX_HPD_HDMI	LA31_N	M2C	LVTTL (VADJ)	Source HPD
D26	TX_HDMI_EN_FPGA	LA26_P	C2M	LVTTL (VADJ)	SN65DP159 OE
G30	CLK_I2C_TX_FPGA_SCL	LA29_P	C2M	LVTTL OD (VADJ)	Source DDC I2C
G31	I2C_TX_FPGA_SDA_OD	LA29_N	BI-DIR	LVTTL OD (VADJ)	
HDMI Sink Signals					
C6	RX_TMDS_DAT0_P	DP0_M2C_P	M2C	TMDS	Sink Channel 0
C7	RX_TMDS_DAT0_N	DP0_M2C_N			
A2	RX_TMDS_DAT1_P	DP1_M2C_P	M2C	TMDS	Sink Channel 1
A3	RX_TMDS_DAT1_N	DP1_M2C_N			
A6	RX_TMDS_DAT2_P	DP2_M2C_P	M2C	TMDS	Sink Channel 2
A7	RX_TMDS_DAT2_N	DP2_M2C_N			
D4	CLK_HDMI_RX_P	GBTCLK0_M2C_P	M2C	LVDS	Sink Clock
D5	CLK_HDMI_RX_N	GBTCLK0_M2C_N			
G18	CLK_I2C_RX_FPGA_SCL	LA16_P	M2C	LVTTL OD (VADJ)	Sink DDC I2C
G19	I2C_RX_FPGA_SDA_OD	LA16_N	BI-DIR	LVTTL OD (VADJ)	
G24	RX_I2C_EN_N_FPGA	LA22_P	C2M	LVTTL (VADJ)	Sink DDC enable
G21	RX_CEC	LA20_P	BI-DIR	LVTTL (VADJ)	Sink CEC
G22	RX_HPD_N	LA20_N	C2M	LVTTL (VADJ)	Sink HPD
G9	SOURCE_DET_N	LA03_P	M2C	LVTTL (VADJ)	Sink detect
Si5324 Clocks					
B20	CLK_MGT_REFCLK_P	GBTCLK1_M2C_P	M2C	LVDS	Si5324 CKOUT1
B21	CLK_MGT_REFCLK_N	GBTCLK1_M2C_N			
H4	CLK_LVDS_P	CLK0_M2C_P	M2C	LVDS	Si5324 CKOUT2

J3 Pin	Schematic Signal Name	VITA 57.1 Name	Direction	Type	Description
H5	CLK_LVDS_N	CLK0_M2C_N	M2C	LVDS	Si5324 CKOUT2
G6	CLKIN_LVDS_P	LA00_CC_P	C2M	LVDS	Si5324 CKIN1
G7	CLKIN_LVDS_N	LA00_CC_N			
C14	REF_CLK_RST_FPGA_N	LA10_P	C2M	LVTTL (VADJ)	Si5324 reset
H7	CLKIN_VALID	LA02_P	M2C	LVTTL (VADJ)	Si5324 INT_C1B
H8	PLL_LOL	LA02_N	M2C	LVTTL (VADJ)	Si5324 LOL
Miscellaneous Signals					
C30	CLK_SCL	SCL	C2M	LVTTL OD	FMC ID EEPROM I2C
C31	SDA_OD	SDA	BI-DIR	LVTTL OD	
G27	CLK_I2C_EE_FPGA_SCL	LA25_P	C2M	LVTTL OD (VADJ)	I2C interface for 64kbit EEPROM
G28	I2C_EE_FPGA_SDA_OD	LA25_N	BI-DIR	LVTTL OD (VADJ)	
H1	Not connected	VREF_A_M2C	M2C		
K1	Not connected	VREF_B_M2C	M2C		
D1	Not connected	PG_C2M	C2M		Not used
F1	10k to VCC_3V3	PG_M2C	M2C		No voltage conditions monitored
H2	0 ohm to GND	PRSNT_M2C_N	M2C	GND	Indicates card present
D29	Not connected	TCK	C2M		
D30	0 ohm to TDO	TDI	C2M		JTAG bypassed
D31	0 ohm to TDI	TDO	M2C		JTAG bypassed
D33	Not connected	TMS	C2M		
D34	Not connected	TRST_N	C2M		
C34	GA0	GA0	C2M	LVTTL	ID EEPROM E1
D35	GA1	GA1	C2M	LVTTL	ID EEPROM E0
J39	VCC_3V3	VIO_B_M2C	M2C	3V3	Provides 3.3V to FPGA Bank B I/O
K40	VCC_3V3	VIO_B_M2C	M2C	3V3	Provides 3.3V to FPGA Bank B I/O
Extender HDMI Source Signals					
A34	EX_TX_CH0_MGT_P	DP4_C2M_P	C2M	CML	SN65DP159 channel 0 input
A35	EX_TX_CH0_MGT_N	DP4_C2M_N			
A38	EX_TX_CH1_MGT_P	DP5_C2M_P	C2M	CML	SN65DP159 channel 1 input
A39	EX_TX_CH1_MGT_N	DP5_C2M_N			
B36	EX_TX_CH2_MGT_P	DP6_C2M_P	C2M	CML	SN65DP159 channel 2 input
B37	EX_TX_CH2_MGT_N	DP6_C2M_N			
B32	EX_CLK_TX_CH3_MGT_P	DP7_C2M_P	C2M	CML	SN65DP159 1 of 2 clock mux input
B33	EX_CLK_TX_CH3_MGT_N	DP7_C2M_N			
C18	EX_CLK_TX_LVDS_P	LA14_P	C2M	LVDS	SN65DP159 2 of 2 clock mux input
C19	EX_CLK_TX_LVDS_N	LA14_N			
D17	EX_TX_CLK_SEL	LA13_P	C2M	LVTTL (VADJ)	SN65DP159 input clock mux select

J3 Pin	Schematic Signal Name	VITA 57.1 Name	Direction	Type	Description
H34	EX_TX_CEC	LA30_P	BI-DIR	LVTTL (VADJ)	Source CEC
H35	EX_TX_HPD_HDMI	LA30_N	M2C	LVTTL (VADJ)	Source HPD
H31	CLK_EX_I2C_TX_SCL	LA28_P	C2M	LVTTL OD (VADJ)	Source DDC I2C
H32	EX_I2C_TX_SDA_OD	LA28_N	BI-DIR	LVTTL OD (VADJ)	
D23	EX_TX_HDMI_EN	LA23_P	C2M	LVTTL (VADJ)	SN65DP159 OE
D8	CLK_EX_I2C_CTL_SCL	LA01_CC_P	C2M	LVTTL OD (VADJ)	I2C for Si5324, EDID EEPROM, and SN65DP159
D9	EX_I2C_CTL_SDA_OD	LA01_CC_N	BI-DIR	LVTTL OD (VADJ)	
Extender HDMI Sink Signals					
A14	EX_RX_TMDS_DAT0_P	DP4_M2C_P	M2C	TMDS	Sink Channel 0
A15	EX_RX_TMDS_DAT0_N	DP4_M2C_N			
A18	EX_RX_TMDS_DAT1_P	DP5_M2C_P	M2C	TMDS	Sink Channel 1
A19	EX_RX_TMDS_DAT1_N	DP5_M2C_N			
B16	EX_RX_TMDS_DAT2_P	DP6_M2C_P	M2C	TMDS	Sink Channel 2
B17	EX_RX_TMDS_DAT2_N	DP6_M2C_N			
H19	CLK_EX_I2C_RX_SCL	LA15_P	M2C	LVTTL OD (VADJ)	Sink DDC I2C
H20	EX_I2C_RX_SDA_OD	LA15_N	BI-DIR	LVTTL OD (VADJ)	
H25	EX_RX_I2C_EN_N	LA21_P	C2M	LVTTL (VADJ)	Sink DDC enable
H22	EX_RX_CEC	LA19_P	BI-DIR	LVTTL (VADJ)	Sink CEC
H23	EX_RX_HPD_N	LA19_N	C2M	LVTTL (VADJ)	Sink HPD
H10	EX_SOURCE_DET_N	LA04_P	M2C	LVTTL (VADJ)	Source detect
Extender Si5324 Clocks					
G2	EX_CLK_LVDS_P	CLK1_M2C_P	M2C	LVDS	Si5324 CKOUT2
G3	EX_CLK_LVDS_N	CLK1_M2C_N			
D20	EX_CLKIN_LVDS_P	LA17_CC_P	C2M	LVDS	Si5324 CKIN1
D21	EX_CLKIN_LVDS_N	LA17_CC_N			
D11	EX_REF_CLK_RST_N	LA05_P	C2M	LVTTL (VADJ)	Si5324 reset
G12	EX_CLKIN_VALID	LA08_P	M2C	LVTTL (VADJ)	Si5324 INT_C1B
G13	EX_PLL_LOL	LA08_N	M2C	LVTTL (VADJ)	Si5324 LOL
Extender Miscellaneous Signals					
H13	EX_PRSNT	LA07_P	M2C	LVTTL (VADJ)	Extender FMC present
D14	CLK_EX_I2C_SCL_VADJ	LA09_P	C2M	LVTTL OD (VADJ)	FMC ID EEPROM I2C
D15	EX_I2C_SDA_VADJ_OD	LA09_N	BI-DIR	LVTTL OD (VADJ)	
H28	CLK_EX_I2C_EE_SCL	LA24_P	C2M	LVTTL OD (VADJ)	I2C interface for 64kbit EEPROM
H29	EX_I2C_EE_SDA_OD	LA24_N	BI-DIR	LVTTL OD (VADJ)	

Notes:

Direction M2C: FPGA Mezzanine Card to FPGA carrier board

Direction C2M: FPGA carrier board to FPGA Mezzanine Card

Direction BI-DIR: Bidirectional

Type OD: Open Drain

8.2. HPC FMC Connector for the Extender TB-FMCH-HDMI4K Card

The HPC FMC connector used to mate to the extender (stacked) FMC uses Samtec ASP-134486-01. Table 8-2 shows the FMC extender connector pin assignment.

Table 8-2 HPC FMC Extender Board Connector Pin Assignment

J8 Pin	Schematic Signal Name	VITA 57.1 Name	Direction	Type	Description
HDMI Source Signals					
C2	EX_TX_CH0_MGT_P	DP0_C2M_P	C2M	CML	SN65DP159 channel 0 input
C3	EX_TX_CH0_MGT_N	DP0_C2M_N			
A22	EX_TX_CH1_MGT_P	DP1_C2M_P	C2M	CML	SN65DP159 channel 1 input
A23	EX_TX_CH1_MGT_N	DP1_C2M_N			
A26	EX_TX_CH2_MGT_P	DP2_C2M_P	C2M	CML	SN65DP159 channel 2 input
A27	EX_TX_CH2_MGT_N	DP2_C2M_N			
A30	EX_CLK_TX_CH3_MGT_P	DP3_C2M_P	C2M	CML	SN65DP159 1 of 2 clock mux input
A31	EX_CLK_TX_CH3_MGT_N	DP3_C2M_N			
C26	EX_CLK_TX_LVDS_P	LA27_P	C2M	LVDS	SN65DP159 2 of 2 clock mux input
C27	EX_CLK_TX_LVDS_N	LA27_N			
C22	EX_TX_CLK_SEL_FPGA	LA18_CC_P	C2M	LVTTL (VADJ)	SN65DP159 input clock mux select
C10	CLK_EX_I2C_CTL_SCL	LA06_P	C2M	LVTTL OD (VADJ)	I2C for Si5324A, EDID EEPROM, and SN65DP159
C11	EX_I2C_CTL_SDA_OD	LA06_N	BI-DIR	LVTTL OD (VADJ)	
G33	EX_TX_CEC	LA31_P	BI-DIR	LVTTL (VADJ)	Source CEC
G34	EX_TX_HPD_HDMI	LA31_N	M2C	LVTTL (VADJ)	Source HPD
D26	EX_TX_HDMI_EN	LA26_P	C2M	LVTTL (VADJ)	SN65DP159 OE
G30	CLK_EX_I2C_TX_SCL	LA29_P	C2M	LVTTL OD (VADJ)	Source DDC I2C
G31	EX_I2C_TX_SDA_OD	LA29_N	BI-DIR	LVTTL OD (VADJ)	
HDMI Sink Signals					
C6	EX_RX_TMDS_DAT0_P	DP0_M2C_P	M2C	TMDS	Sink Channel 0
C7	EX_RX_TMDS_DAT0_N	DP0_M2C_N			
A2	EX_RX_TMDS_DAT1_P	DP1_M2C_P	M2C	TMDS	Sink Channel 1
A3	EX_RX_TMDS_DAT1_N	DP1_M2C_N			
A6	EX_RX_TMDS_DAT2_P	DP2_M2C_P	M2C	TMDS	Sink Channel 2
A7	EX_RX_TMDS_DAT2_N	DP2_M2C_N			
G18	CLK_EX_I2C_RX_SCL	LA16_P	M2C	LVTTL OD (VADJ)	Sink DDC I2C
G19	EX_I2C_RX_SDA_OD	LA16_N	BI-DIR	LVTTL OD (VADJ)	
G24	EX_RX_I2C_EN	LA22_P	C2M	LVTTL (VADJ)	Sink DDC enable
G21	EX_RX_CEC	LA20_P	BI-DIR	LVTTL (VADJ)	Sink CEC
G22	EX_RX_HPD_N	LA20_N	C2M	LVTTL (VADJ)	Sink HPD
G9	EX_SOURCE_DET_N	LA03_P	M2C	LVTTL (VADJ)	Source detect
Si5324 Clocks					
H4	EX_CLK_LVDS_P	CLK0_M2C_P	M2C	LVDS	Si5324 CKOUT2

J8 Pin	Schematic Signal Name	VITA 57.1 Name	Direction	Type	Description
H5	EX_CLK_LVDS_N	CLK0_M2C_N			
G6	EX_CLKIN_LVDS_P	LA00_CC_P	C2M	LVDS	Si5324 CKIN1
G7	EX_CLKIN_LVDS_N	LA00_CC_N			
C14	EX_REF_CLK_RST_N	LA10_P	C2M	LVTTL (VADJ)	Si5324 reset
H7	EX_CLKIN_VALID	LA02_P	M2C	LVTTL (VADJ)	Si5324 INT_C1B
H8	EX_PLL_LOL	LA02_N	M2C	LVTTL (VADJ)	Si5324 LOL
Miscellaneous Signals					
C30	CLK_EX_I2C_SCL	SCL	C2M	LVTTL OD	FMC ID EEPROM I2C
C31	EX_I2C_SDA_OD	SDA	BI-DIR	LVTTL OD	
G27	CLK_ EX_I2C_EE_SCL	LA25_P	C2M	LVTTL OD (VADJ)	I2C interface for 64kbit EEPROM
G28	EX_I2C_EE_SDA_OD	LA25_N	BI-DIR	LVTTL OD (VADJ)	
H1	Not connected	VREF_A_M2C	M2C		
K1	Not connected	VREF_B_M2C	M2C		
D1	Not connected	PG_C2M	C2M		
F1	Not connected	PG_M2C	M2C		
H2	EX_PRSNT	PRSNT_M2C_N	M2C	VADJ	Indicates card present
D29	Not connected	TCK	C2M		
D30	Not connected	TDI	C2M		
D31	Not connected	TDO	M2C		
D33	Not connected	TMS	C2M		
D34	Not connected	TRST_N	C2M		
C34	GA0	GA0	C2M	LVTTL	ID EEPROM E1
D35	GA1	GA1	C2M	LVTTL	ID EEPROM E0
J39	Not connected	VIO_B_M2C	M2C		
K40	Not connected	VIO_B_M2C	M2C		

Notes:

Direction M2C: FPGA Mezzanine Card to FPGA carrier board

Direction C2M: FPGA carrier board to FPGA Mezzanine Card

Direction BI-DIR: Bidirectional

Type OD: Open Drain

8.3. HDMI Connectors

The HDMI connectors use Samtec HDMR-19-01-S-SM.

Table 8-3 shows the HDMI Source connector (J1) pin assignments and Table 8-4 shows the HDMI Sink connector (J2) pin assignments.

Table 8-3 HDMI Source Connector (J1)

Pin #	Schematic Signal Name	Pin Name	Description
1	TX_TMDS_DAT2_P	TMDS_DATA2_P	TMDS transmit data 2+
2	GND	TMDS_SHLD2	TMDS transmit data 2 shield
3	TX_TMDS_DAT2_N	TMDS_DATA2_N	TMDS transmit data 2-
4	TX_TMDS_DAT1_P	TMDS_DATA1_P	TMDS transmit data 1+
5	GND	TMDS_SHLD1	TMDS transmit data 1 shield
6	TX_TMDS_DAT1_N	TMDS_DATA1_P	TMDS transmit data 1-
7	TX_TMDS_DAT0_P	TMDS_DATA0_P	TMDS transmit data 0+
8	GND	TMDS_SHLD0	TMDS transmit data 0 shield
9	TX_TMDS_DAT0_N	TMDS_DATA0_N	TMDS transmit data 0-
10	CLK_TX_TMDS_P	TMDS_CLK_P	TMDS transmit clock+
11	GND	TMDS_CLK_SHLD	TMDS transmit clock shield
12	CLK_TX_TMDS_N	TMDS_CLK_N	TMDS transmit clock-
13	CEC_SOURCE	CEC	CEC signal
14	UTI	RSVD/HEC_DATA_N	Reserved/HEC-
15	CLK_I2C_TX_DDC_SCL	DDC_SCL	DDC serial clock
16	I2C_TX_DDC_SDA_OD	DDC_SDA	DDC serial data
17	GND	DDC/CEC GND	DDC/CEC ground
18	None (connected, but no net name assigned)	DDC_5V	+5V power supply
19	HPD_IN	HOTPLUG_DET/HEC_DATA_P	Hot-plug detection/HEC+

Table 8-4 HDMI Sink Connector (J2)

Pin #	Schematic Signal Name	Name	Description
1	RX_TMDS_D2_P	TMDS_DATA2_P	TMDS receive data 2+
2	GND	TMDS_SHLD2	TMDS receive data 2 shield
3	RX_TMDS_D2_N	TMDS_DATA2_N	TMDS receive data 2-
4	RX_TMDS_D1_P	TMDS_DATA1_P	TMDS receive data 1+
5	GND	TMDS_SHLD1	TMDS receive data 1 shield
6	RX_TMDS_D1_N	TMDS_DATA1_P	TMDS receive data 1-
7	RX_TMDS_D0_P	TMDS_DATA0_P	TMDS receive data 0+
8	GND	TMDS_SHLD0	TMDS receive data 0 shield
9	RX_TMDS_D0_N	TMDS_DATA0_N	TMDS receive data 0-
10	CLK_RX_TMDS_P	TMDS_CLK_P	TMDS receive clock+
11	GND	TMDS_CLK_SHLD	TMDS receive clock shield
12	CLK_RX_TMDS_N	TMDS_CLK_N	TMDS receive clock-
13	CEC_SINK	CEC	CEC signal
14	Not connected	RSVD/HEC_DATA_N	Reserved/HEC-
15	CLK_I2C_RX_SCL	DDC_SCL	DDC serial clock
16	I2C_RX_SDA_OD	DDC_SDA	DDC serial data
17	GND	DDC/CEC GND	DDC/CEC ground
18	VCC_5V0_RX	DDC_5V	+5V power supply
19	HPD_OUT	HOTPLUG_DET/HEC_DATA_P	Hot-plug detection/HEC+

The receiver has an EEPROM (ST Microelectronics M24C64-WDW6TP), which is used to store EDID data. The EDID EEPROM is accessed on the same I2C bus that is used for control of the SN65DP159 and the Si5324 at address 0b1010000x.

Note: At factory default settings, the EDID EEPROM stores temporary data to enable output of image data from an image output device. The ID used in the data is a dummy ID for evaluation purposes. Do not use it for actual products.

9. I2C Busses

9.1. FMC I2C EEPROM

A 2kbit I2C EEPROM (M24C02) is provided for FMC identification, as described in section 5.5 of ANSI/VITA 57.1. It is at I2C address 0b1010000x and is connected to the FMC dedicated I2C pins at J3-C30 (SCL) and J3-C31 (SDA). The pull-up resistors to 3V3_AUX are not populated (R205 and R206) since the pull-ups should be provided on the main board. The EEPROM is permanently enabled for writing.

The FMC identification EEPROM for the extender card is connected to J3-D14 (LA09_P) for SCL and J3-D15 (LA09_N) for SDA. These signals are connected to J8-C30 (SCL) and J8-C31 (SDA) via a PCA9517 I2C bus repeater.

The FMC identification EEPROM is programmed at the factory to enable automated identification,

verification, and configuration of Main Board parameters. The contents of the EEPROM are available in Appendix A: FMC I2C EEPROM Contents.

Note: The user must be cognizant that the FMC I2C EEPROM is always write-enabled. As it contains critical information required for correct operation, one must never overwrite the factory settings.

9.2. I2C Control Bus

An I2C control bus interfaces to the SN65DP159, the Si5324, and the M24C64 64kbit HDMI Sink EDID EEPROM. It is connected to the main board FMC connector at J3-C10 (LA06_P) for SCL and J3-C11 (LA06_N) for SDA. A PCA9517 I2C bus repeater is used to provide voltage translation. It has 10kohm pull-up resistors on the FMC connector side to VADJ.

Table 9-1 I2C Control Bus

Device	I2C Address	Device SCL Pin	Device SDA Pin
SN65DP159	0b1011110x	U20-13	U20-14
Si5324	0b1101000x	U52-22	U52-23
M24C64	0b1010000x	U19-6	U19-5

9.3. Future EEPROM I2C Bus

There is an I2C bus dedicated for a 64kbit M24C64 EEPROM. The EEPROM is at address 0b1010000x. The connection to the J3 main board FMC connector is through a PCA9517 I2C bus repeater, with 10kohm pull-up resistors to VADJ on the connector side. The SCL clock line is connected to J3-G27 (LA25_P) and the SDA data line is connected to J3-G28 (LA25_N). There are no other devices on this I2C bus. The EEPROM is permanently enabled for writing.

Connections are provided for the future EEPROM on the extender HDMI4k card. The J3 main board FMC connector has SCL at J3-H28 (LA24_P) and SDA at J3-H29 (LA24_N).

The main purpose of the future EEPROM is for data storage to enable HDCP encryption. If not used for this purpose it may be used for any other non-volatile data storage purpose.

9.4. HDMI DDC

The HDMI DDC (Display Data Channel) interface is implemented for both the Source and Sink HDMI ports. A bypass loopback is also provided using four 3-pin headers. Figure 9-1 illustrates the connections for the Source and Sink.

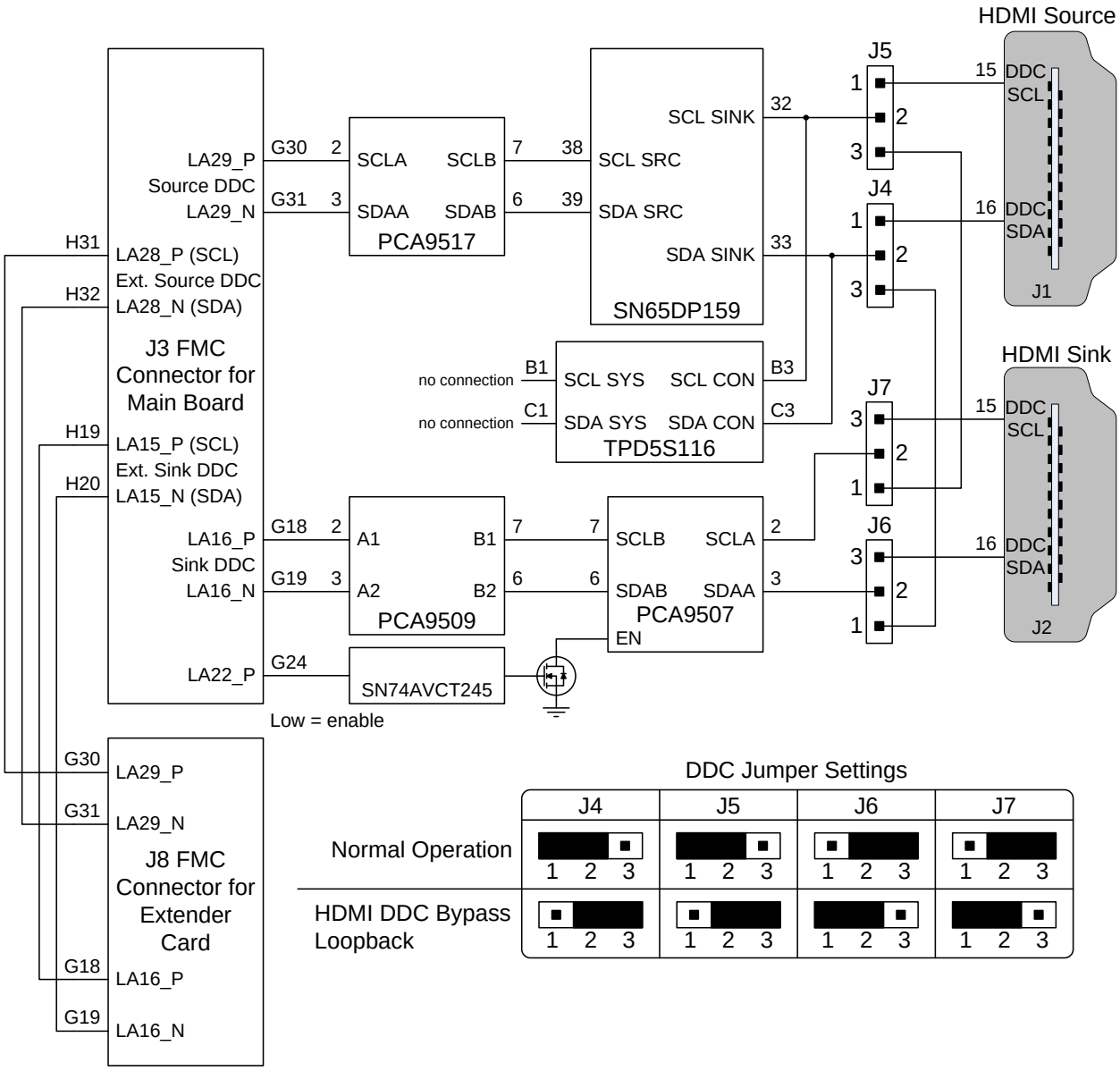


Figure 9-1 HDMI Source and Sink DDC

The TB-FMCH-HDMI4K is shipped with the J4, J5, J6, and J7 jumpers placed in the normal operation positions. They can be moved for test purposes. The source DDC connections to the TPD5S116 are for ESD protection and provide pull-up resistors. J3-G24 (LA22_P) should be low to enable the sink DDC.

10. Clocks

10.1. Si5324 Any-Frequency Clock Generator

The Silicon Labs Si5324C Any-Frequency Precision Clock Multiplier/Jitter Attenuator enables the user to generate the desired video clock frequency for use by the FPGA. An onboard 114.285 MHz crystal can be used to asynchronously generate the video clocks. The CKIN1 differential input from the FPGA can

also be used to synchronously generate the video clocks. The CKIN2 input is not used. Figure 10-1 shows how the Si5324 is connected to the main board and how the extender FMC Si5324 is connected. Please refer to the Si5324 data sheet for how to set the registers to produce the desired clocks.

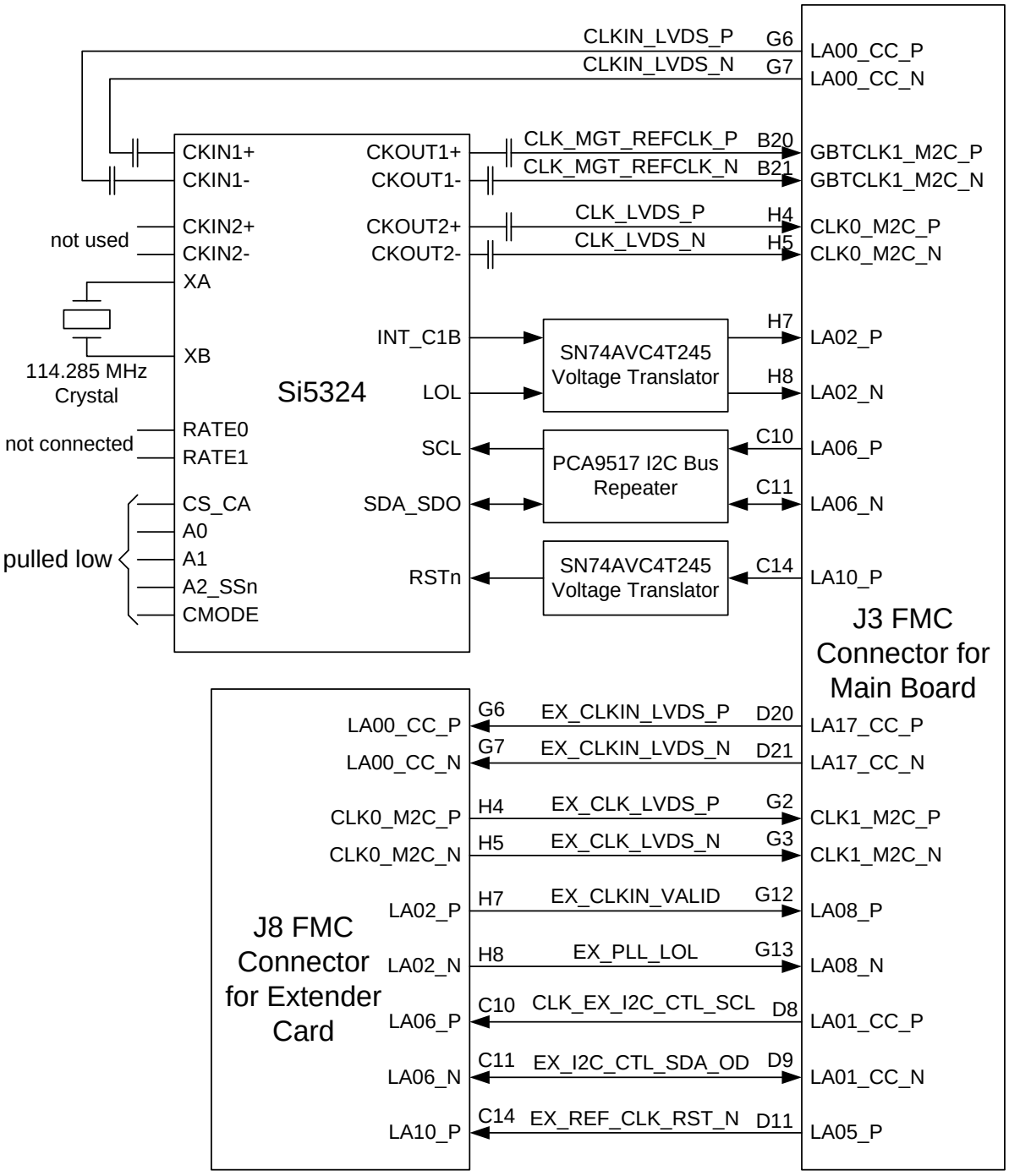


Figure 10-1 Si5324A Clock Generator

Note: Due to I/O limitations on the J3 Main Board FMC connector, the stacked FMC's Si5324 clock generator only provides EX_CLK_LVDS_P/N to the J8 connector.

10.2. HDMI Source Clock

The SN65DP159 drives the HDMI source TMDS differential clock using the clock from its IN_CLKp/n input. A Texas Instruments TS3USB221 1:2 multiplexer is used to feed IN_CLKp/n. This allows a choice

of two source clocks from the FPGA.

Figure 10-2 shows how the clocks are connected and how the extender FMC clocks are connected.

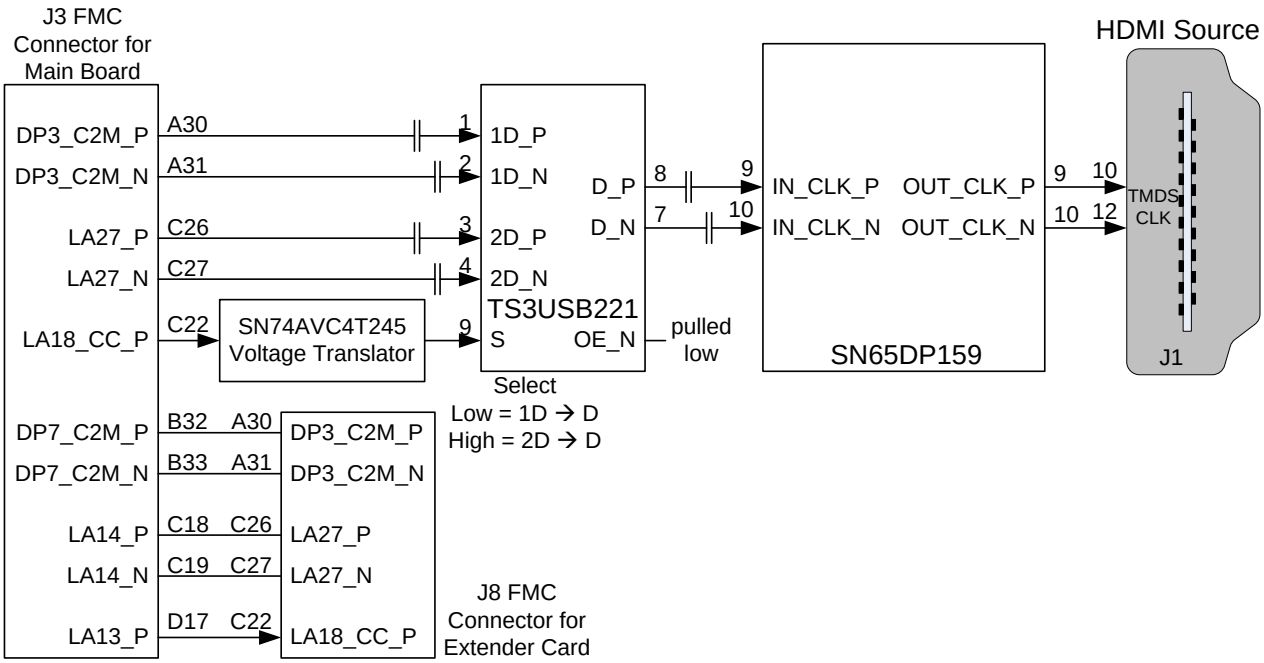


Figure 10-2 HDMI Source Clocks

10.3. HDMI Sink Clock

The HDMI TMDS sink clock is terminated and AC coupled to a DS90LV001 LVDS buffer. The buffer output is AC coupled to the GBTCLK0_M2C input clock of the J3 FMC main board connector (J3-D4, J3-D5). The LVDS buffer is permanently enabled.

11. Hot Plug Detect (HPD)

The HDMI sink HPD signal is controlled via a MOSFET. The MOSFET control signal is from J3-G22 (LA20_N) through a voltage translator. The sink HPD signal is low when LA20_N is high. It is also connected to the HPD connector input of a Texas Instruments TPD5S116 HDMI companion chip for transient protection.

The HDMI source HPD signal from the J1 HDMI source connector connects to the HPD connector input of another TPD5S116. The TPD5S116 HPD system output connects to J3-G34 (LA31_N). The source HPD signal also connects to the HPD Sink input of the SN65DP159. This enables the SN65DP159 to know when the HPD signal is active.

Two three-pin headers (J11 and J13) provide a bypass loopback for test purposes. Figure 11-1 shows how the HPD signals are connected and how the extender FMC HPD signals are connected.

Note: The TB-FMCH-HDMI4k does not support the HDMI Ethernet and Audio Return Channel (HEAC) on either HDMI interface.

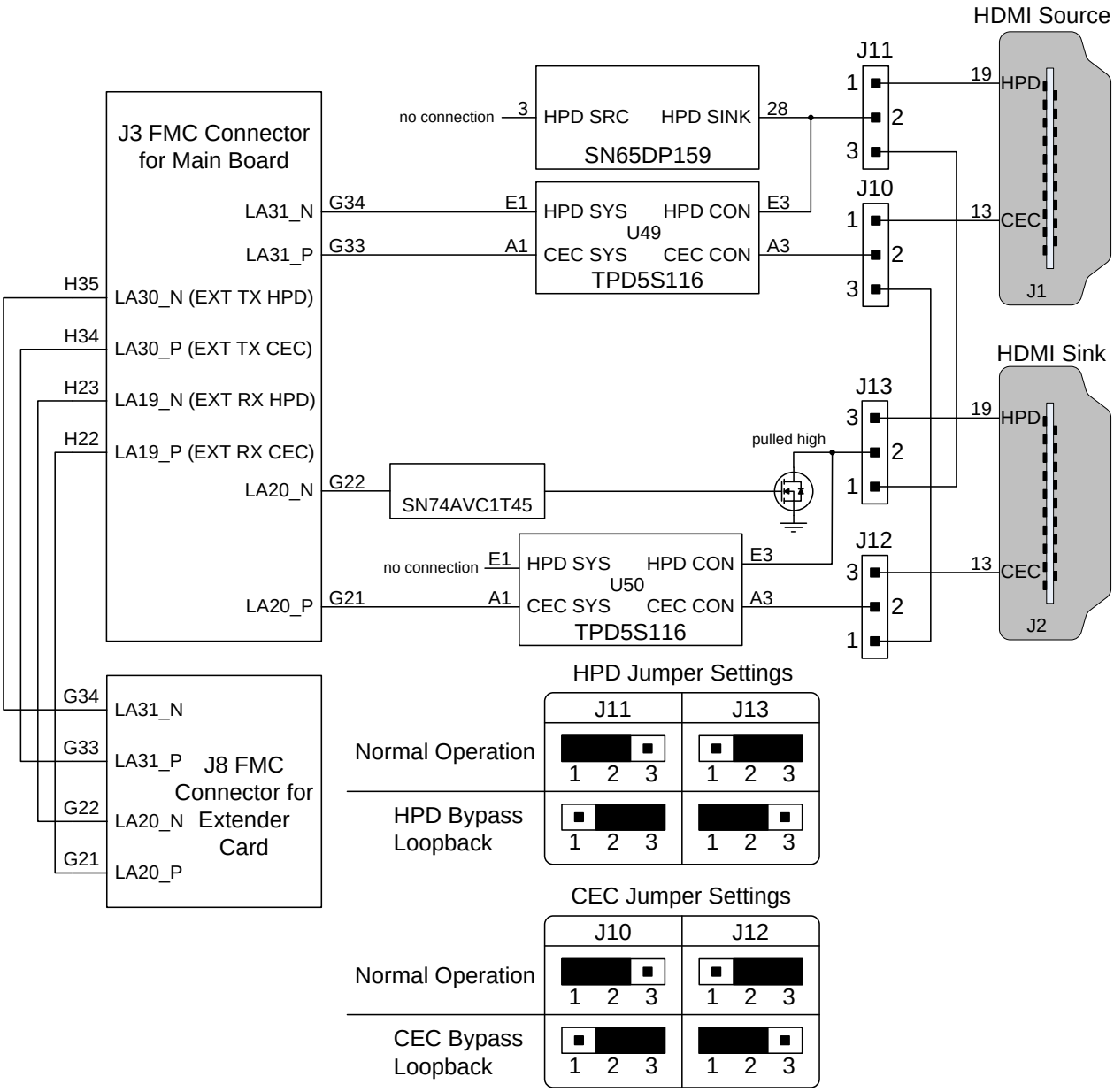


Figure 11-1 HDMI HPD and CEC Connections

12. Consumer Electronics Control (CEC)

The HDMI sink and source CEC signals pass through two Texas Instruments TPD5S116 companion chips. This provides voltage translation, ESD protection, and terminations. Two three-pin headers (J10 and J12) provide a bypass loopback for test purposes. Figure 11-1 shows how the CEC signals are connected and how the extender FMC CEC signals are connected.

13. ESD Protection

All HDMI source and sink TMDS differential signals are protected with Texas Instruments TPD1E05U06DPYT unidirectional ESD protection devices. They provide IEC 61000-4-2 level 4

protection and are designed for HDMI 2.0, as well as for other high speed interfaces. IEC 61000-4-2 level 4 ESD protection for the single-ended HDMI source and sink signals is provided by two Texas Instruments TPD5S116 HDMI companion chips.

14. Test Points

There are 12 test points accessible on the component side of the card. This includes four through-hole ground test points and eight test point pads for voltage rails. Table 14-1 lists all the test points and shows the locations of the test points. Note that TP1, TP2, and TP8 do not exist.

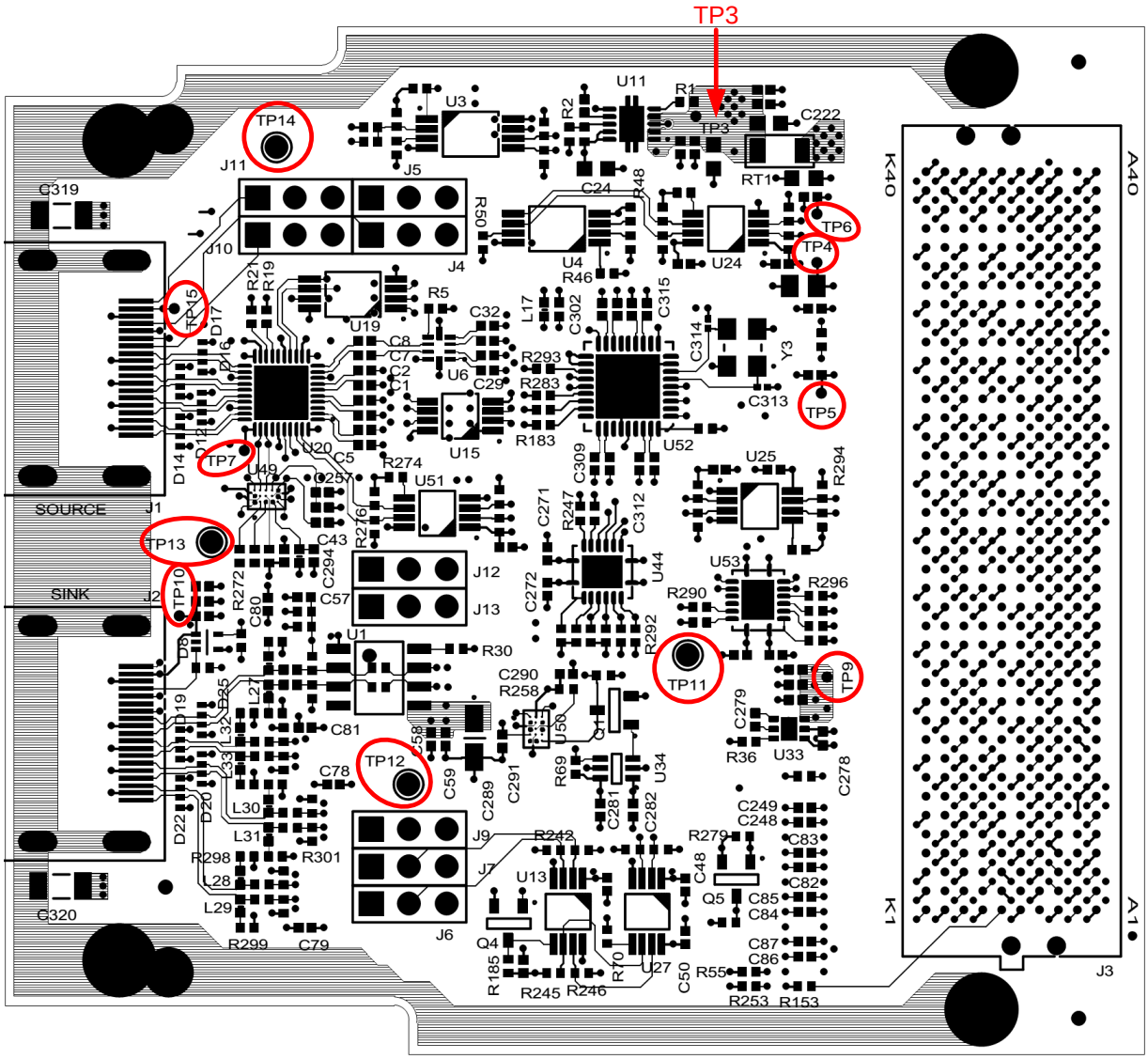


Figure 14-1 Test Point Locations on Component Side

Table 14-1 Test Points

Test Point	Schematic Signal Name	Nominal Voltage	Component Pin
TP3	VCC_3V3	3.3V	U11-1, 2
TP4	VCC_12V	12.0V	J3-C35, C37
TP5	3V3_AUX	3.3V	J3-D32
TP6	FMC_VADJ	1.2V to 3.3V	J3-E39, F40, G39, H40
TP7	VCC_1V1	1.1V	U11-9, 10
TP9	VCC_5V0	5.0V	U33-3
TP10	VCC_5V0_RX	5.0V	J2-18
TP11	GND	ground	---
TP12	GND	ground	---
TP13	GND	ground	---
TP14	GND	ground	---
TP15	---	5.0V	J1-18, U49-D3

15. Demonstration

The latest HDMI reference design is provided by Xilinx.

The reference design is made available to registered users via Xilinx's "HDMI Lounge". To register, please email Xilinx at video_ref_design@xilinx.com and request access to the "HDMI Lounge".

For any questions regarding the reference design, please first review the online technical support information at: http://www.xilinx.com/support/service-portal.html . If your question is not addressed in the online forums, consider submitting a Xilinx online technical support request.

16. Appendix A: FMC I2C EEPROM Contents

The following table describes the contents of the FMC I2C EEPROM as programmed at the factory.

Table 16-1 FMC I2C EEPROM Contents

Board Information

Field	Size	Data
Language Code	1	0
Date / Time of Manufacture	3	<Variable>
Board Manufacturer	16	FidusSystemsInc
Board Product Name	16	TB-FMCH-HDMI4K
Board Serial Number	16	<Variable>
Board Part Number	16	PA-10077-01
FRU File ID	1	0
Hardware Revision	6	<Variable>
MAC Address	6	00:00:00:00:00:00

Multi-Record Information

VITA Subtype 0 Record

Field	Size	Data	Description
Vendor OUI	3	0x0012A2	Fixed value of 0x0012A2
Subtype/Version	1	0x00	7:4 (type): main definition type 3:0 (version): current version
Size/Connectors/Clock Dir	1	0x1C	7:6 (size): single width 5:4 (P1 size): HPC 3:2 (P2 size): not fitted 1 (clock dir): Mezzanine to Carrier 0: reserved 0
P1 Bank A Number Signals	1	0x31	49 signals
P1 Bank B Number Signals	1	0x00	
P2 Bank A Number Signals	1	0x00	
P2 Bank B Number Signals	1	0x00	
P1/P2 Number Transceivers	1	0x80	7:4 (P1 GBT): 8, 3:0 (P2 GBT): 0
Max Clock for TCK	1	0x95	In units of MHz: 149MHz

DC Load Record – VADJ

Field	Size	Data	Description
Output Information	1	0x00	Bit map containing output number, etc. (VADJ)
Nominal Voltage	2	0x00B4	In units of 10mV (1.8V)
Minimum Voltage	2	0x0078	In units of 10mV (1.2V)
Maximum Voltage	2	0x014A	In units of 10mV (3.3V)
Ripple and Noise (PK-PK)	2	0x0032	In units of 1mV (10Hz to 30MHz) (50mV)
Minimum Current Draw	2	0x0005	In units of 1mA (5mA)
Maximum Current Draw	2	0x0078	In units of 1mA (120mA)

DC Load Record – 3P3V

Field	Size	Data	Description
Output Information	1	0x01	Bit map containing output number, etc. (3.3V)
Nominal Voltage	2	0x014A	In units of 10mV (3.3V)
Minimum Voltage	2	0x0139	In units of 10mV (3.13V)
Maximum Voltage	2	0x0154	In units of 10mV (3.4V)
Ripple and Noise (PK-PK)	2	0x0032	In units of 1mV (10Hz to 30MHz) (50mV)
Minimum Current Draw	2	0x00FA	In units of 1mA (250mA)
Maximum Current Draw	2	0x07D0	In units of 1mA (2.0A)

DC Load Record – 12P0V

Field	Size	Data	Description
Output Information	1	0x02	Bit map containing output number, etc. (12V)
Nominal Voltage	2	0x04B0	In units of 10mV (12V)
Minimum Voltage	2	0x0474	In units of 10mV (11.4V)
Maximum Voltage	2	0x04EC	In units of 10mV (12.6V)
Ripple and Noise (PK-PK)	2	0x0064	In units of 1mV (10Hz to 30MHz) (100mV)
Minimum Current Draw	2	0x0000	In units of 1mA
Maximum Current Draw	2	0x0000	In units of 1mA

DC Output Record – VIO_B_M2C

Field	Size	Data	Description
Output Information	1	0x03	Bit map containing output number, etc.
Nominal Voltage	2	0x014A	In units of 10mV (3.3V)
Minimum Voltage	2	0x0139	In units of 10mV (3.13V)
Maximum Voltage	2	0x0154	In units of 10mV (3.4V)
Ripple and Noise (PK-PK)	2	0x0032	In units of 1mV (10Hz to 30MHz) (50mV)
Minimum Current Load	2	0x0000	In units of 1mA
Maximum Current Load	2	0x03E8	In units of 1mA (1.0A)

DC Output Record – VREF_A_M2C

Field	Size	Data	Description
Output Information	1	0x04	Bit map containing output number, etc.
Nominal Voltage	2	0x0000	In units of 10mV
Minimum Voltage	2	0x0000	In units of 10mV
Maximum Voltage	2	0x0000	In units of 10mV
Ripple and Noise (PK-PK)	2	0x0000	In units of 1mV (10Hz to 30MHz)
Minimum Current Load	2	0x0000	In units of 1mA
Maximum Current Load	2	0x0000	In units of 1mA

DC Output Record – VREF_B_M2C

Field	Size	Data	Description
Output Information	1	0x05	Bit map containing output number, etc.
Nominal Voltage	2	0x0000	In units of 10mV
Minimum Voltage	2	0x0000	In units of 10mV
Maximum Voltage	2	0x0000	In units of 10mV
Ripple and Noise (PK-PK)	2	0x0000	In units of 1mV (10Hz to 30MHz)
Minimum Current Load	2	0x0000	In units of 1mA
Maximum Current Load	2	0x0000	In units of 1mA

17. Appendix B: Headers, Factory Default, and Orientation

The following depicts the factory default header jumper positions and clarifies the pin numbering and orientation of the headers.

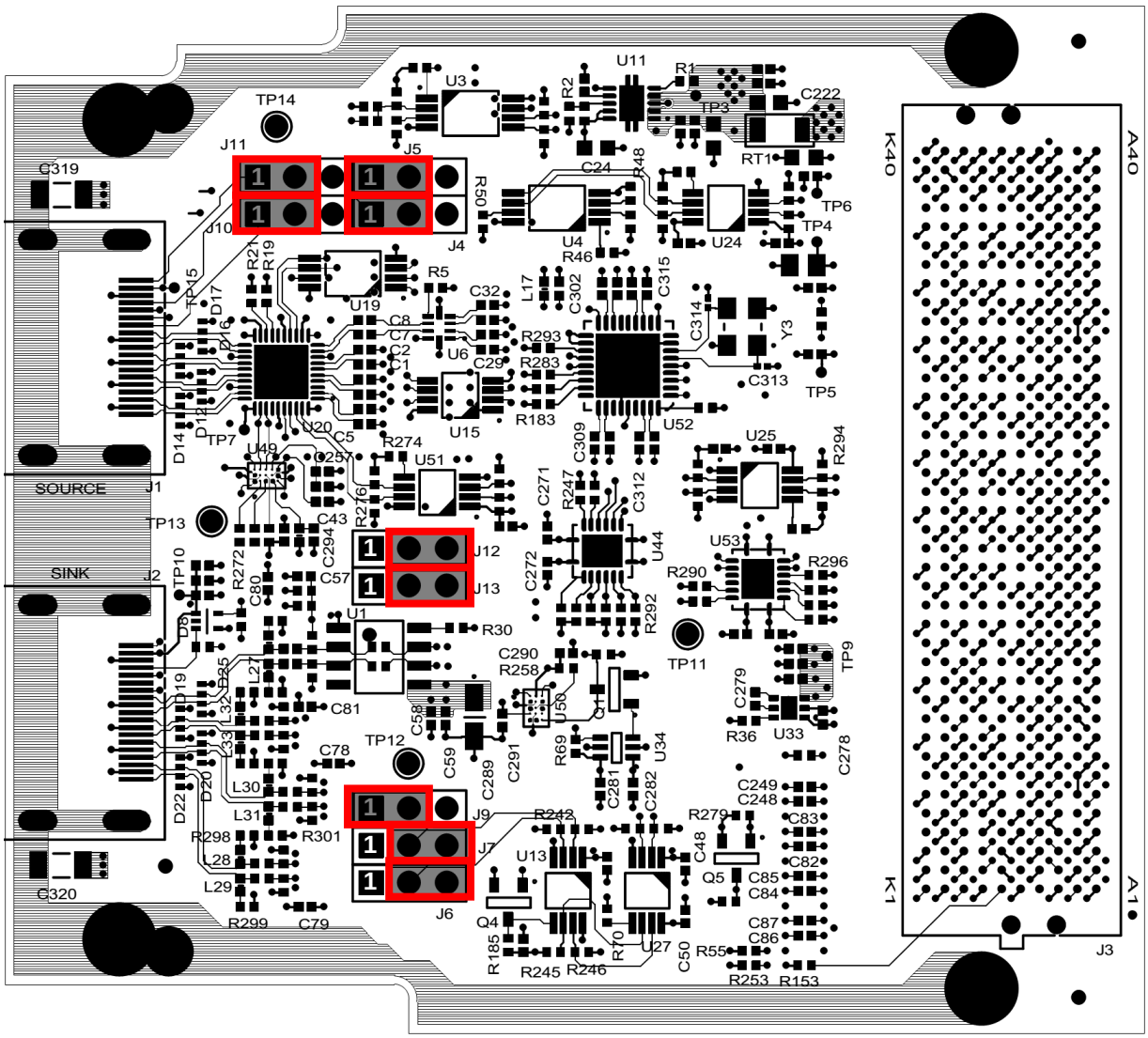


Figure 17-1 Default Jumper Positions and Header Orientation

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